High Performance Off-Line Switch Mode Power Supply

INTRODUCTION

Within the next year, the Switch Mode Power Supply (SMPS) market is expected to grow from 30% to well over 50% of the power supply business. Users are demanding low cost and high reliability in a smaller, lighter package, and recent advances in the development of high voltage power FETs are having a significant impact on the design of SMPS's. The IVN6000KNT has several unique characteristics ideal for SMPS applications. Clever utilization of these qualities results in substantial system gains over traditional bipolar designs.

450 VOLT VERTICAL POWER MOS FET

Fabrication

The IVN6000 family is fabricated in Intersil's new vertical DMOS process. "Self-aligned" processing (with fewer masking operations and no critical etching) eliminates many of the manufacturing and reliability problems which plagued the prior art. A cross section of the vertical DMOS structure is shown in Figure 1.

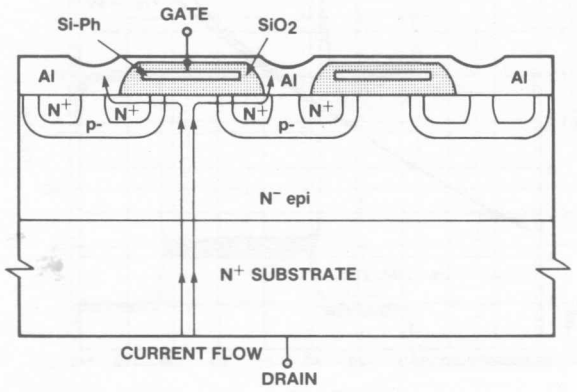

Figure 1. Vertical DMOS Structure

The surface topology of the IVN6000KNT has been designed for maximum breakdown voltage and drain current while minimizing capacitance and switching time for a given chip size.

Power MOS FETs offer significant performance/cost advantages over bipolar power transistors in many applications. A comparison of devices is shown in Table 1.

Safe Operating Area Rating (SOAR)

The Safe Operating Area curve for the IVN6000KNT is shown in Figure 2.

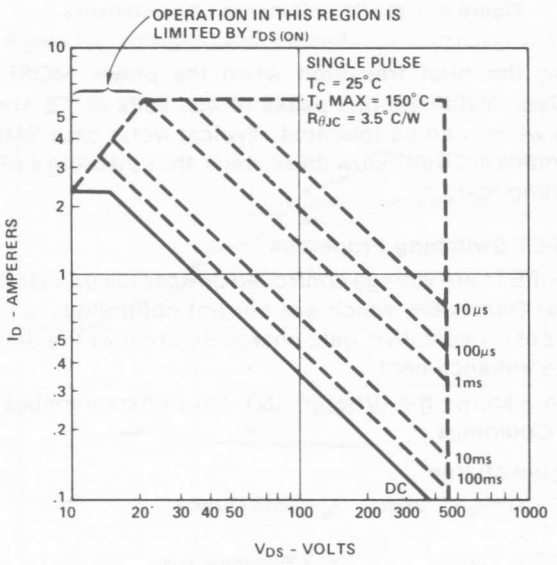

Figure 2. Safe Operating Area (SOA)

Table 1.

POWER FET	BIPOLAR
Advantages	**Advantages**
1. Wide Safe Operating Area (SOA)	1. Low Saturation Voltage
2. Very High Current Gain	2. Availability
3. Very Fast Switching	
4. "Free" Reverse Diode	
5. No Thermal Runaway	
6. Drive Simplicity	
7. Inherent Current-sharing when paralleled	
Disadvantages	**Disadvantages**
1. Static Sensitivity	1. Device Storage Time — Losses, Frequency Limitations
2. Comparatively High Conduction Losses	2. Base Drive Complexity and Power Dissipation
	3. Current Hogging when Paralleled
	4. Thermal Runaway
	5. SOA Limitations

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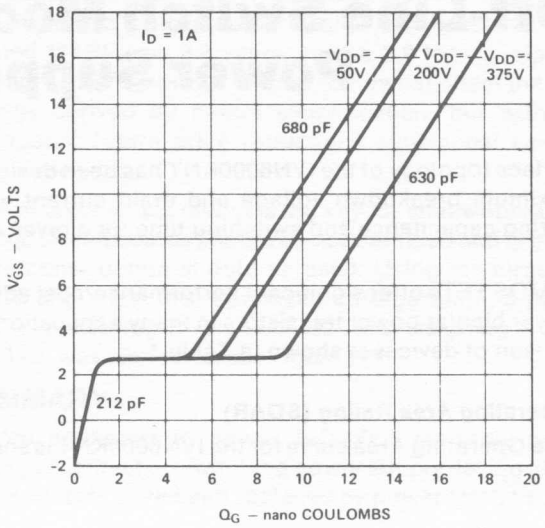

Figure 3. Gate Drive Dynamic Characteristics

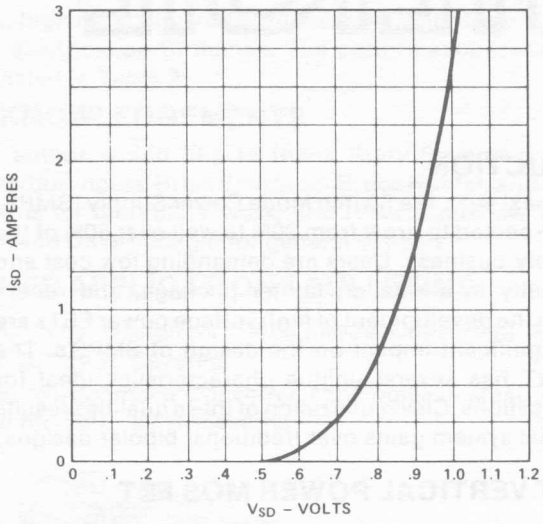

Figure 4. Diode Forward Voltage Characteristics

During the brief transition when the power MOSFET switches, instantaneous peaks of 450 volts at 7.5 amps (3375 watts) can be tolerated. Typical worst case SMPS conditions are well below these limits, thus insuring a wide operating margin.

MOSFET Switching Properties

Power FETs are voltage controlled devices (as opposed to bipolar transistors which are current controlled). Since the input is capacitive, gate charge determines the drain-source enhancement.

Figure 3 shows the IVN6000KNT drive characteristics in nano Coulombs.

Since the charge

$Q = I_g t_s$ where I_g = Gate Current

then

$t_s = Q/I_g$ t_s = Switching Time

The switching time is dictated almost entirely by the applied gate current since there is no minority carrier storage time.

Switching a 1 A load to 375 Volts in 100 nanoseconds requires only 100 milliamperes of gate drive. This feature makes possible the use of extremely simple and reliable drive circuits, as well as operation far in excess of the traditional 20 kHz switching frequency.

Integral Reverse Diode

Inherent in the power MOSFET is a fast recovery epitaxial diode with very acceptable low forward drop. This "free" reverse diode serves an important role in many SMPS topologies. During the time interval in which the power MOSFET is off, the reverse diode provides a path for inductor current. Bipolar designs require the addition of an "extra" discrete fast-recovery diode. The IVN6000KNT integral reverse diode is fast and also exhibits low loss. The diode forward drop characteristics are shown in Figure 4.

Under typical operation, a forward drop of < 1.0 Volt is common.

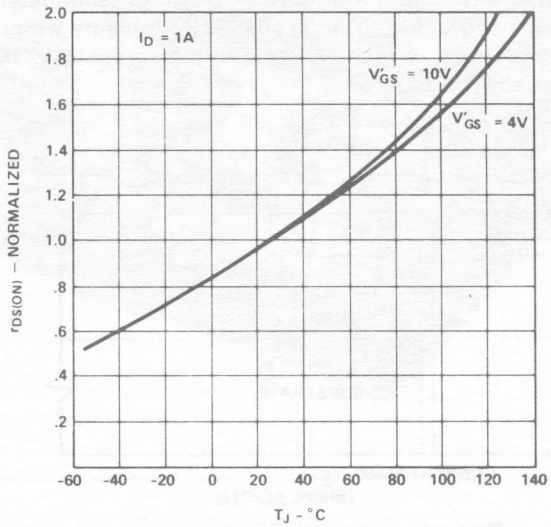

Figure 5. ON Resistance vs. Junction Temperature ($V'_{GS} = V_{GS} - V_{GS(th)}$)

Paralleling MOSFETs

The IVN6000KNT can be paralleled without fear of current hogging or thermal runaway. This is significant in that it allows the designer to scale up/down designs by merely paralleling devices. The device has a positive temperature coefficient for $r_{DS(on)}$. See Figure 5.

The device conduction losses are

$P_c = V_{DS}^2/r_{DS(on)}$ where V_{DS} = Drain-source on voltage

$r_{DS(on)}$ = Drain-source on resistance

Given the situation in which two paralleled devices have different $r_{DS(on)}$ values, the device with lower ON resistance will dissipate the most power. Junction heating increases $r_{DS(on)}$ and reduces its power dissipation, and this negative-feedback insures stable operation between paralleled devices.

DESIGN NOTES

The complete 5V/50 Amp off-line (100/220 VAC) SMPS using power MOSFETs is shown in Figure 6. The system specifications are as follows:

SPECIFICATIONS:

Input Characteristics:	115/220 + 10%-20% VAC, 47-63 Hz
DC Output Ratings:	5V at 50A
Output Ripple and Noise:	50 mV_{pp} Maximum
Overload Protection:	Fold-back type with automatic recovery
Over Voltage Protection:	Set at 5.6V
Temperature Rating:	Operating 0°C to +40°C at full-rated power
Cooling:	Convection
Thermal Protection:	Internal thermostat shutdown for over temperature
Remote Sensing:	Available to provide compensation for line losses.
AC Under Voltage Inhibit:	Inhibits operation below 90/180 volts AC input
Slow Turn-On Circuitry:	In-rush current limiting thermistor, slow-start pulse width modulation

Power Mesh

The converter configuration chosen for this application was the half bridge. As illustrated in App. Note A034, other topologies may result in lower conduction losses, however, the half bridge has several advantages. A prime consideration is that maximum voltage seen across the FETs cannot exceed the rail voltage. For 110/220 VAC line this represents a peak of 360 VDC. However, to insure sufficient guard banding to accommodate line/rail spikes and low temperature BV_{DSS} de-rating, the IVN6000KNT —450 volt power FET is recommended. The half bridge is also advantageous in terms of the transformer design. A smaller core, without primary center-tap, and a favorable turns ratio are derived.

Other key factors in selecting this topology were:

1. Well-understood and easy-to-stabilize feedback loop.
2. Relatively low RFI.
3. Circuit simplicity — single transformer driver, utilization of the FET integral reverse rectifier.

An operating frequency of 60 kHz (per switch) was chosen. This is a compromise in that only modest improvements in size, weight, bandwidth, etc., are derived as a direct result. The major improvements are achieved through circuit simplification. The criterion for selecting this frequency was the availability of components; i.e., diodes, capacitors, integrated circuits, etc.

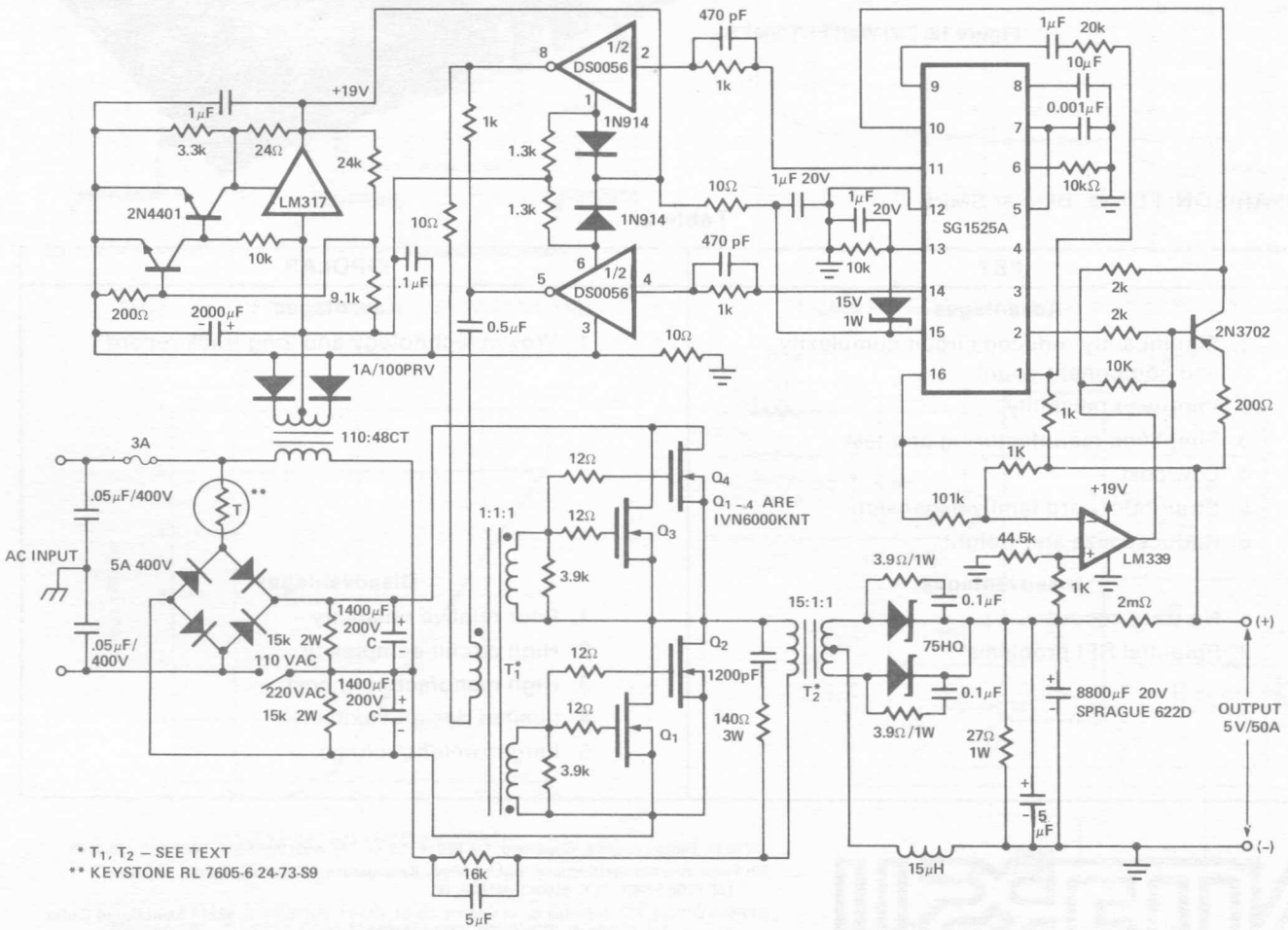

Figure 6. Power MOSFET SMPS

The output is straightforward, consisting of a full wave center-top configuration and LC filter. 75HQ Schottky rectifiers are used to reduce rectifier dissipation. Worst case losses for the Schottky diodes is 35 watts.

The half bridge consists of two pairs of IVN6000KNTs. Paralleling limits the conduction losses to a maximum of six watts/FET or 24 watts total. Each device sees less than 1.25A RMS and 2A peak, well within the rated 2.25A RMS and 7.5A peak.

The power transformer consists of a single primary and center tapped secondary, with a turns ratio of 15:1:1. To achieve high efficiency it is important to keep the magnetizing and leakage losses low. It can be shown that a magnetizing current $I_m = 0.4A$ results in a worst case increased dissipation of 3W (total). This being acceptable, the minimum magnetizing inductance L_m becomes:

$$L_m = \frac{V_t}{I} \quad \text{or} \quad L_m \sim 4.5\ \text{mH}$$

Losses due to leakage inductance must also be minimized since:

$$P_{LK} = L_{LK} \times I_p^2 \times F$$

Paying close attention to the magnetic design, L_{LK} as low as 4.5 μH can be achieved. This results in a maximum leakage loss $P_{LK} \sim 3.7$ watts. The RC snubber network absorbs most of this energy. Core and copper losses account for about 2.5 watts. A ferrite, toroidal core was chosen with filar windings; this structure tends to reduce leakage inductance and RFI.

FET Driver

Of first order is the switching losses. The energy dissipated during the switching interval is:

$$W_S = \int_0^t V_{DS}(t)\, I_D(t)\, dt$$

The switching losses can then be expressed as:

$$P_S = \left[f_S W_{S(on)} + W_{S(off)} \right]$$

Assuming constant current and linear voltage ramps, the expression for the switching losses becomes:

$$P_S \sim f_S \times V_{DS} \times I_D \times t_S$$

A more exact expression for switching losses can be derived, however the contribution of losses due to switching is small in comparison to other system losses.

Acceptable switching losses are obtained when the switching time is 40ns; i.e., $P_s = 0.75$ watt/device. The gate drive current required to achieve a t_s of 40ns is

$$I_g = \frac{Q_g}{t_s}$$

where

$Q_g \sim$ 10 nano Coulombs/device

or

$I_g \sim 0.25$A/device

This is derived with the DS0056, high speed, monolithic dual clock driver, which provides up to 1.5A at 20 volts output drive. Drive transformer T_1 is tri-filar wound 1:1:1 with a magnetizing inductance $L_m \sim 7$mH and leakage inductance $L_{LK} \sim 0.7\ \mu$H. Minimization of L_{LK} is essential. It can be shown that L_{LK} dominates in the calculation of switching time where:

$$t_s \approx \sqrt{\frac{2\, Q_g\, L_{LK}}{V_{DT}}}$$

and

$V_{DT} = V_{DRIVER} - V_{TH}$ 10 or $t_s \sim 37$ ns.

This drive configuration has several advantages. Foremost is the condition that both outputs can never be on simultaneously. (Such a condition could be destructive to the FETs.) Furthermore, when power is removed, both outputs drop to zero rapidly, preventing any voltage spikes or asymmetrical charging. The circuit operates Class-C, consuming power only when an output is high. These functions are concisely achieved with a total of 10 components.

Switching Regulator Subsystem

Many of the basic characteristics of the power supply are controlled by the regulator subsystem. The circuit shown in Figure 6 uses an SG1525A integrated circuit to provide output regulation via duty cycle variation of the drive signal to the DS0056's. The SG1525A provides the required reference voltage on pin 16, the operating frequency of the system is controlled by the oscillator components on pins 5 and 7, and the circuit provides an automatic slow-start function through the capacitor on pin 8. Overvoltage protection is achieved by allowing the 2N3702 to activate the shutdown circuitry at pin 10. Frequency compensation is controlled by the components between pins 1 and 9, which set the medium frequency dynamic performance of the supply and also the loop stability. The LM339 and associated resistors provide short circuit current limiting with fold-back. (Note that the SG1525, which can be used in the same circuit, has a slightly different pin out.)

More complicated control functions can be realized by replacing the LM339 with devices such as the SG1542 through SG1544. Somewhat improved dynamic response can be achieved by using the TL494 in place of the SG1525A, and incorporating feed-forward compensation. This device also includes a current limiting circuit, obviating the need for the LM339, as shown in Figure 11.

Input Circuitry

The input circuitry is standard. A thermistor limits the in-rush current, and a shorting clip allows the option of 110 VAC or 220 VAC; a 3-terminal pass regulator provides power for the controller and driver; a 2-transistor, resistor network coupled to the LM317 provides "under voltage" protection. The auxiliary supply is regulated to 19 volts.

SYSTEM PERFORMANCE

Figure 7 is an oscillograph depicting the power transformer voltage and current waveforms. Figure 8 displays the voltage waveforms in the half bridge. The actual FET gate-source and drain-source waveforms are expanded in Figure 9. Current limiting is the fold-back type. The resulting output characteristics are illustrated in Figure 10.

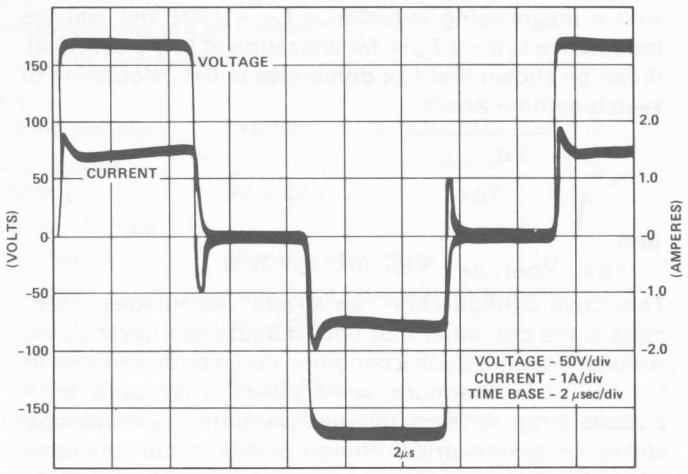

Figure 7a. Voltage/Current Waveforms Across T_2. 25A Load.

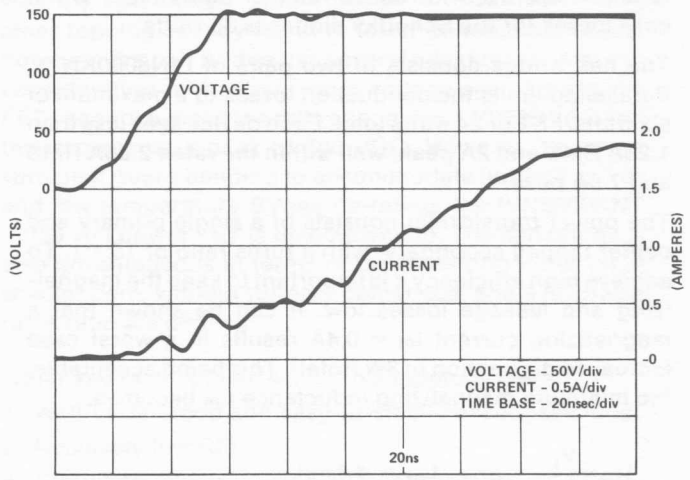

Figure 7b. Voltage/Current Waveforms Expanded. 25A Load.

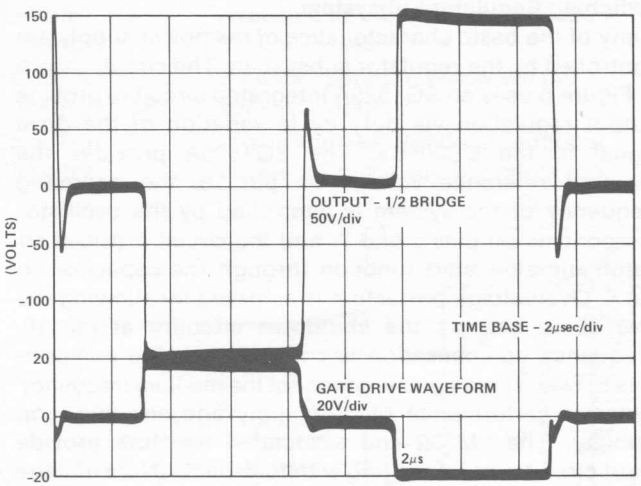

Figure 8. Half Bridge Waveforms (5V/25A Load)

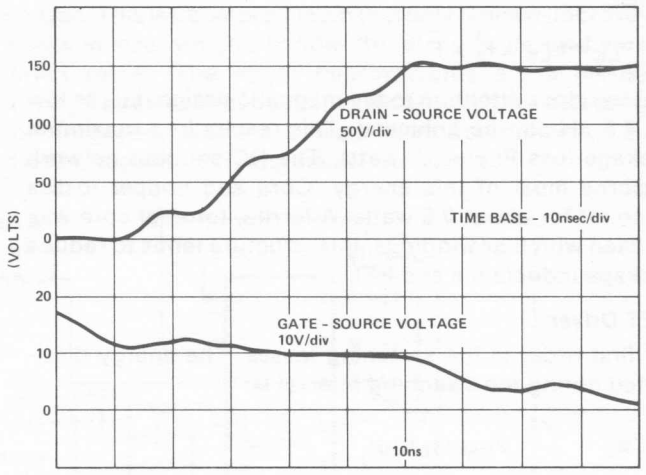

Figure 9. FET Switching Waveforms (5V/25A Load)

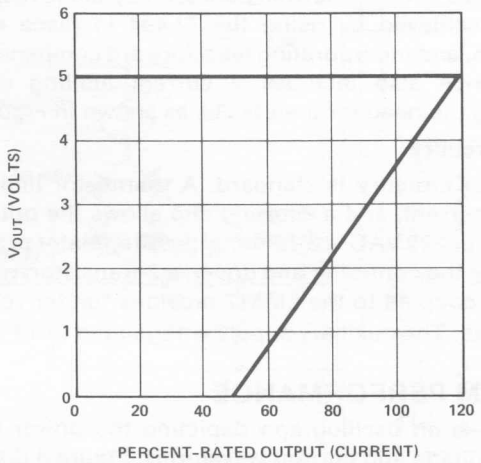

Figure 10. Current Fold-Back Characteristics

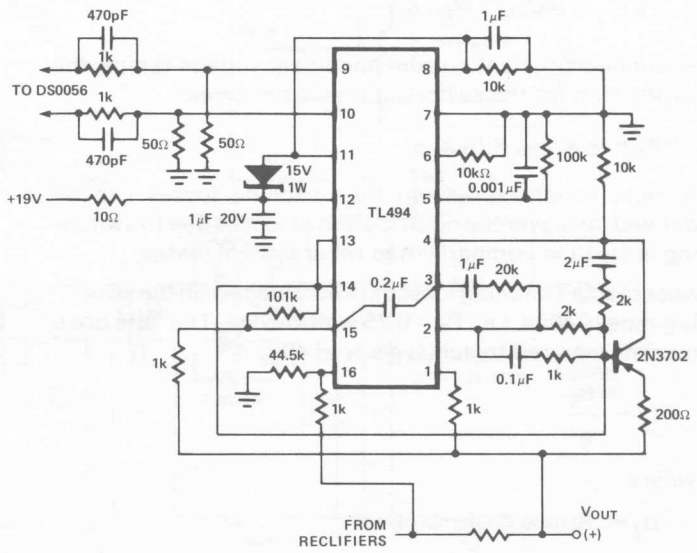

Figure 11. Alternative Control Circuit

The complete SMPS has a total of about 90 circuit elements, compared to a typical bipolar design which has 140. Calculated MTBF was 3.7 years, versus 2.9 for the bipolar. Current MOSFET prices tend to somewhat offset the cost savings derived by circuit simplification, but with the anticipated future price reductions substantial savings can be realized.

A clean mechanical layout is the key for stable operation; printed circuit boards should be double sided and ground-plane construction should be used. Using the circuit of Figure 6 in a far from optimized configuration, a power supply measuring 6" x 9" x 3-1/2" and weighing a mere 4 lb. 4 oz. was fabricated, see Figure 12.

SUMMARY

Recent advances in power MOSFET technology are having an impact on switching power supply design. Bipolar transistors have been replaced by power MOS FETs to achieve significant system advantages including lower cost, high reliability, reduced size and weight, and excellent electrical performance. The performance trade-offs are listed in Table 2.

ACKNOWLEDGEMENTS

The author would like to thank Rudy Severns for his numerous inputs; Brian Smithson, Bruce Hunter, and Janis Jenkins for laboratory work; and Peter Bradshaw, Larry Goff, and Dave Fullagar for general support.

OTHER APPLICATIONS BULLETINS

A034, *"The Design of Switchmode Converters Above 100kHz,"* by R. Severns.

A035, *"Switchmode Converter Topologies — Make Them Work for You,"* by R. Severns.

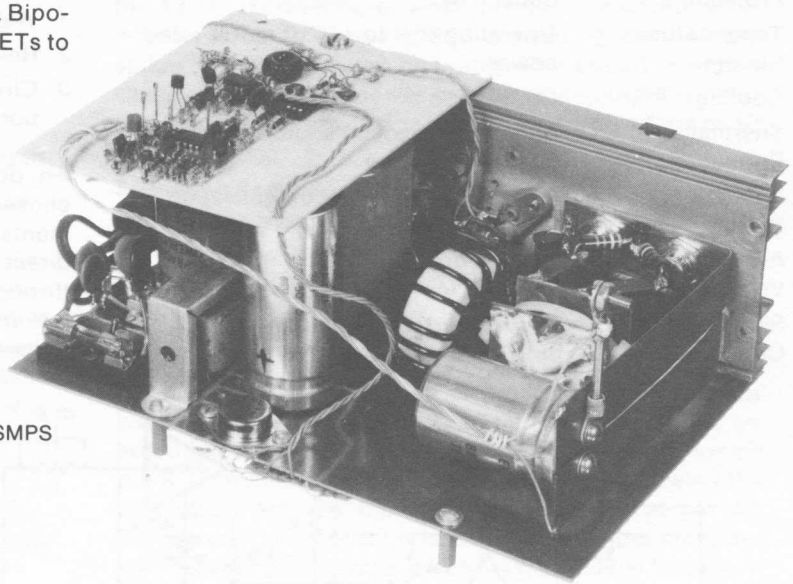

Figure 12. 250 Watt FET SMPS

COMPARISON: FET vs. Bipolar SMPS

Table 2.

FET	BIPOLAR
Advantages	**Advantages**
1. Significantly reduced circuit complexity and component count	1. Proven technology and long track record
2. Improved reliability	
3. Simplified manufacturing and test	
4. Low cost	
5. Straightforward family expansion	
6. Reduced size and weight	
Disadvantages	**Disadvantages**
1. No track record	1. Poor relative reliability
2. Potential RFI problems	2. High circuit complexity
	3. High manufacturing cost
	4. Limited design flexibility
	5. Larger weight/volume

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